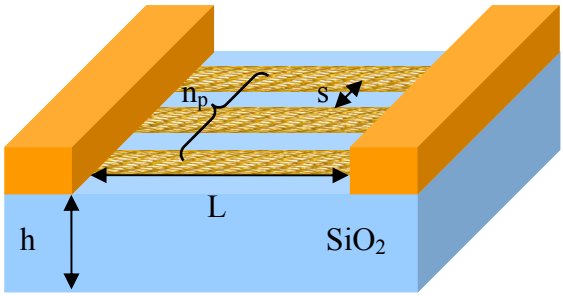
CNT-Interconnect Verilog-A Model User Guide

This model is developed and tested using the Cadence Spectre environment [1].

Please refer to the Verilog-A user guide for further guidance on Verilog-A simulations [2].



Circuit Diagram (for a couple of CNT-wires)

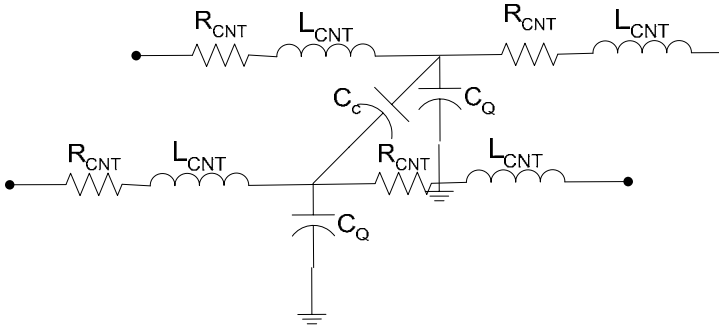


Table 1: Verilog-A parameters for interconnect model

Parameter	**Description**	**Default Parameters**
Instance Parameters		
d	Diameter	1nm
np	Number of CNT's in parallel	1
S	Spacing between CNT's	10nm
eins	Dielectric constant of insulator	25
Cc	Coupling capacitance	0
h	Substrate insulator thickness	100nm
L	wire length	100nm
Model Parameters		
phisb	Schottky barrier height	0eV
Vcrit*	Energy for optical-phonon scattering parameter	0.16eV
Rp/Rn	Parasitic access resistance	0 ohm
lacc*	Mfp for acoustic phonon scattering	1.0um
lzb*	Mfp for zone boundry phonon scattering	20nm

*These are the fitting parameters.

Parameter Tuning Procedure

Step 0: Define instance parameters. (Note: The model calculates a simple coupling capacitance based on geometry. If the user wishes to use 2D or 3D solvers like Raphael to calculate C_c the calculated value can be overrided using the parameter Cc and setting Cflag to 1. Otherwise set Cflag to 0.

Step 1: If 'L' ranges between 10nm and 1um, tune Vcrit in the range of 0.08 to 0.16 to decrease the resistance. If L> 1um, acoustic phonon scattering dominates and therefore lacc will change the slope of the curve.

Step 2: If the contacts are short and ohmic then Rs and Rd can be ignored. At high current values the phisb value can be extracted.

Instructions to Setup the Model in Spectre

1. Create any two-terminal symbol in Cadence with pins p,n.
2. Create a Verilog A cellview. (Design > Create Cellview > from Cellview > Tool/Datatype = Verilog-A Editor.
3. Copy the Verilog-A file into the directory created by step 2. Overwrite the existing file. The name of the file should be verilog.va.
4. Setup the device parameters and fitting parameters as mentioned in the Readme file and you are ready to run standard simulations in Spectre.

References

[1] Virtuoso® Spectre® circuit simulator user guide, Version 5.1.41, August 2004.

[2] Cadence® Verilog® -A Language Reference Manual, Version 5.0, July 2002.