CNT Verilog-A model User Guide

This is a User Guide for the Verilog-A model available for download at

http://www.eas.asu.edu/~ptm/cnt

This model is developed and tested using the Cadence Spectre environment [1].

Refer to the Verilog-A user guide for further guidance on Verilog-A simulations [2]

Procedure for CNT Model Setup in Spectre:

1. Create a four-terminal symbol as shown in Fig. 1 (Any four-terminal device symbol will work) with the pins as d,g,s,b.

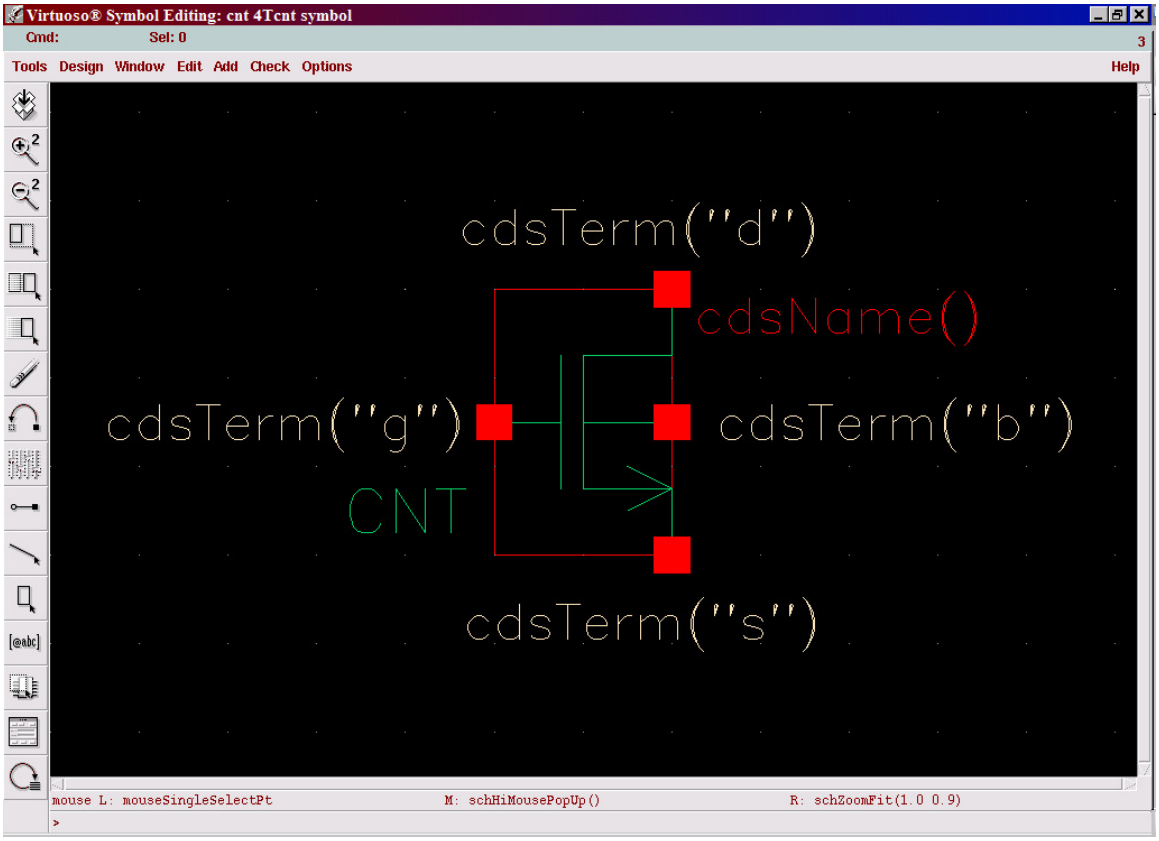

Fig. 1: CNT Symbol

2. Create a Verilog-A cellview. (Design -→ Create Cellview →from Cellview →Tool/Datatype = Verilog-A Editor.

3. Copy the Verilog-A file (verliloga.va) and the chirality lookup table (NN_table.tbl) to the veriloga directory created by following Step 2. (Do not change the name, overwrite the default file.)

4. The table 1 gives the device parameters. They are divided into Instance parameters and model parameters

Table 1: Verilog-A parameters

Parameter	**Description**	**Default Parameters**
Instance Parameters		
d	Diameter	1nm
θ	Chiral angle(0< θ<30)	0
tins	Insulator thickness	10nm
eins	Dielectric constant of insulator	25
tback	Substrate insulator thickness	100nm
eback	Substrate insulator Dielectric constant	3.9
L	Gate length	100nm
Type	N-type =1 or p-type=-1	1
Model Parameters		
phisb	Schottky barrier height	0eV
Mob*	Scattering parameter (mobility degradation)	1
Rs/Rd	Parasitic access resistance	0
β*	Coupling coefficient (empirical)	20
Cc	Coupling Capacitance	7aF/μm
Csubfit*	Flat band correction factor	1
Cp*	Parasitic capacitance	0aF/μm

*These are the fitting parameters.

5. Instance parameters are all the physical parameters of the device. The table also lists the defaults set in the code.

6. DC Simulation: Run a standard simulation as shown in Fig 2 using the default parameters.

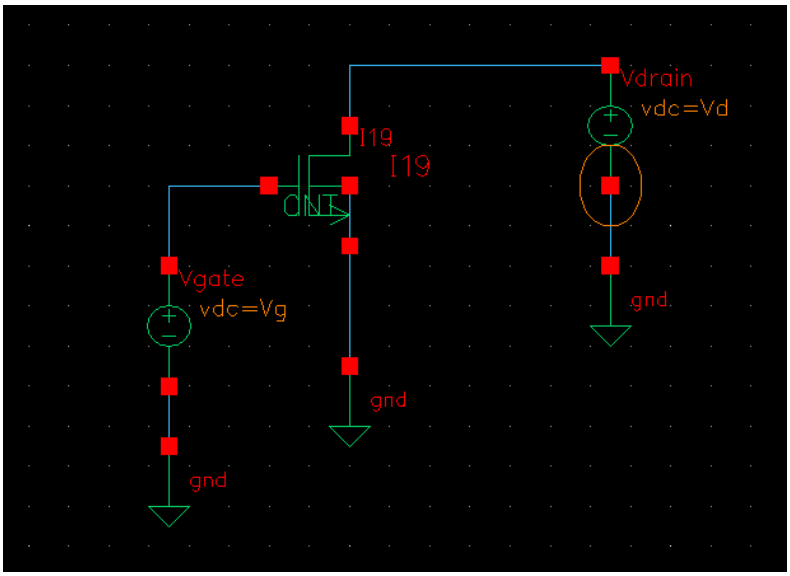

Fig. 2: DC Simulation

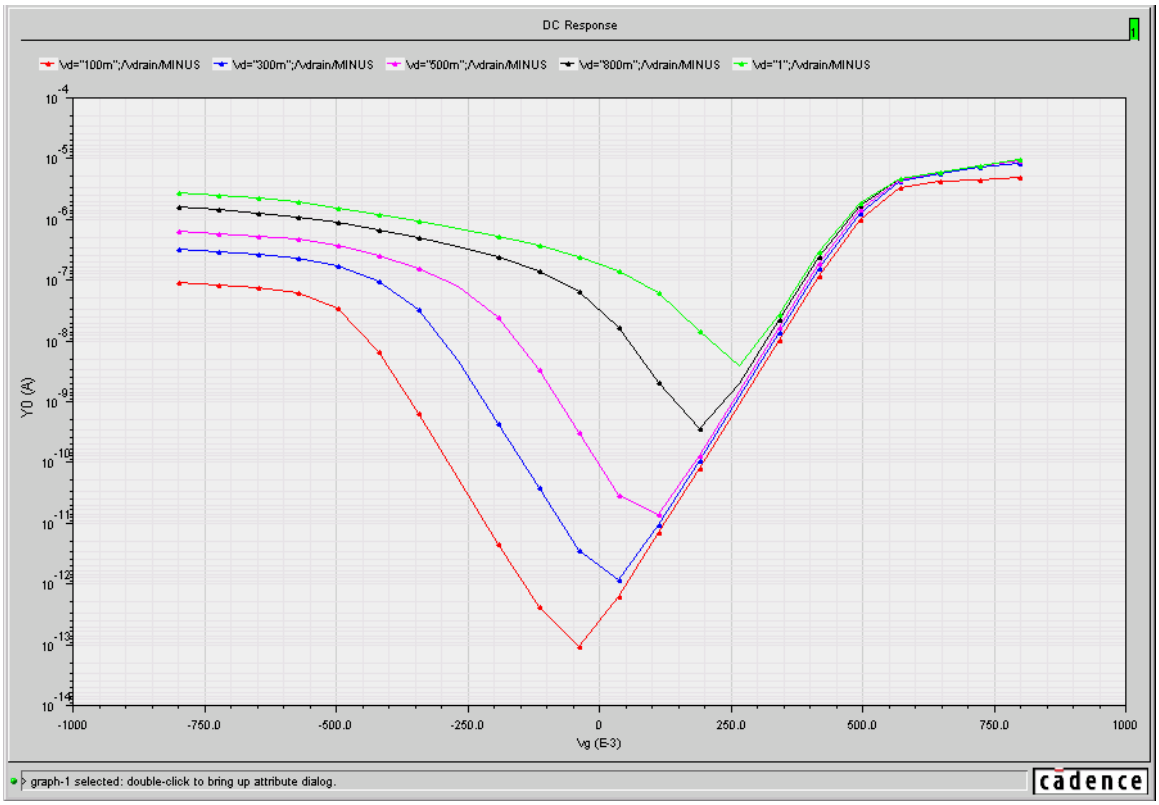

Fig. 3: I_{DS} vs. V_{GS} for V_{DS} =0.1V, 0.3V, 0.5V, 0.8V, 1V.This is the result with the default parameters

7. Five fitting parameters are used to match the data.

The fitting procedure is as follows:

Step 0: define instance parameters; calculate physical parasitics (Cc is set to a very small value, which is about 1/10 of the insulator capacitance)

Step 1: Csubfit: tuned to fit I_{DS} vs. V_{GS}, at low V_{DS} (~0.1V) , with fixed VBS fixed. This is to match the flat bland voltage.

Step 2: Beta: tuned to fit Ids vs. V_{DS} at a high V_{GS}, to match the saturation region (basically the shape of the Ids vs. V_{DS} curve)

Step 3: Cp: tuned to match I_{DS} vs. V_{GS} in the subthreshold region, at high V_{DS}; sometimes, Phisb also needs to be tuned to match I_{DS} vs. V_{GS} in the saturation region.

Step 4: R_{DS}: tuned to match I_{DS} vs. V_{DS} in the linear region

Step 5: Mob: used to match the saturated drain current

References:

[1] Virtuoso® Spectre® circuit simulator user guide, Version 5.1.41, August 2004.

[2] Cadence® Verilog® -A Language Reference Manual, Version 5.0, July 2002.